Design of Power Factor Correction Circuit Using AP1662

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1. Introduction

The AP1662 is an active power factor control IC which is designed mainly for use as a pre-converter in electronic ballasts, AC-DC adapters and off-line SMPS applications. The AP1662 includes an internal start-up timer for stand-alone applications, a one-quadrant multiplier to realize near unity power factor and a zero current detector to ensure DCM boundary conduction operation. The totem pole output stage is capable of driving Power MOSFET with 600mA source current and 800mA sink current.

Designed with the advanced BiCMOS process, the AP1662 features low start-up current, low operation current and low power dissipation. The AP1662 also has rich protection features including over-voltage protection, input under-voltage lockout with hysteresis and multiplier output clamp to limit maximum peak current.

2. Product Features

- Zero Current Detection Control for DCM Boundary Conduction Mode
- Adjustable Output Voltage with Precise Over-Voltage Protection
- Low Start-up Current with 40μA Typical Value
- Low Operating Supply Current with 2.5mA Typical Value
- 1% Precise Internal Reference Voltage
- Internal Start-up Timer
- Disable Function for Reduced Current Consumption
- Totem Pole Output with 600mA Source Current and 800mA Sink Current
- Under-Voltage Lockout with 2.5V of Hysteresis

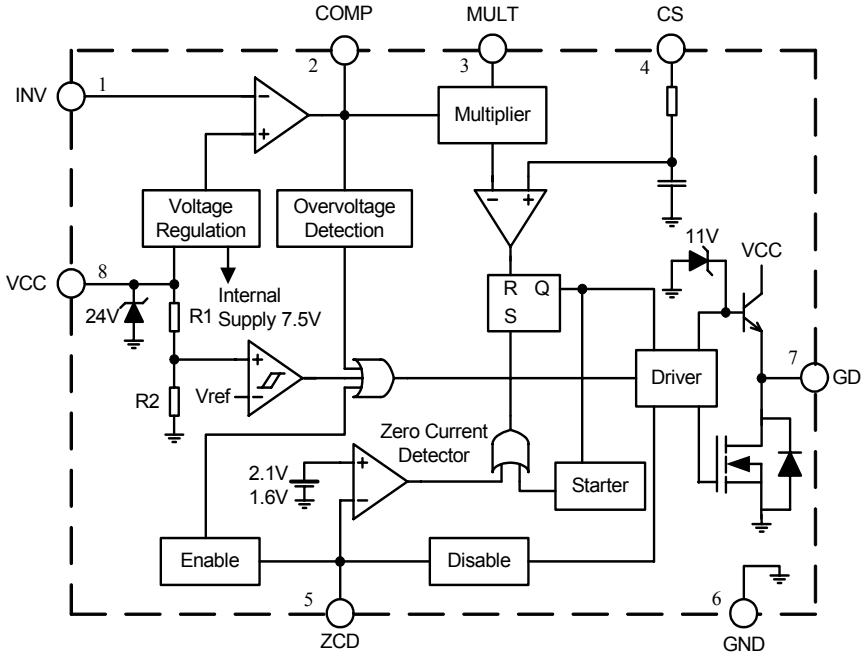

Figure 1. Functional Block Diagram of AP1662

3. Pin Descriptions

INV (Pin 1): This pin is the inverting input of the error amplifier. It is connected to an external resistor divider which senses the output voltage.

COMP (Pin 2): This pin is the error amplifier output, it is made available for voltage loop compensation by resistor and capacitor combination between pin 1 and this pin.

MULT (Pin 3): Input of the multiplier. This pin senses the AC sinusoidal voltage and is multiplied with the COMP pin voltage.

CS (Pin 4): Input of the current control comparator. This pin senses the power switch current and meashures it against the output of the multiplier. When the CS pin voltage is higher than the output of the multiplier, the gate driver signal will become low to turn off the external MOSFET.

ZCD (Pin 5): Zero current detection input. When the ZCD pin voltage decreases below 1.6V, the gate drive signal becomes too high to turn on the external MOSFET. If it is connected to GND, the device is disabled.

GND (Pin 6): Ground. Current return for gate driver and control circuits of the IC.

GD (Pin 7): Gate driver output. A series resistor between this pin and the power switch gate can reduce high frequency noise.

VCC (Pin 8): Supply voltage of gate driver and control circuits of the IC.

4. Functional Block Descriptions

Supply Block

As shown in Figure 2, pin 8 is the VCC of AP1662. There is a zener diode with typical 24V clamp voltage (30 mA rated) to protect the device. A voltage regulator generates a 7.5V voltage to function as the IC's internal supply. It also produces a precise internal reference voltage (2.5V±1% at 25°C)

A hysteresis comparator detects the VCC pin's voltage. As long as the VCC voltage is high enough, the driver is enabled. To start the AP1662, the VCC voltage must exceed the start-up threshold voltage (13V max.).

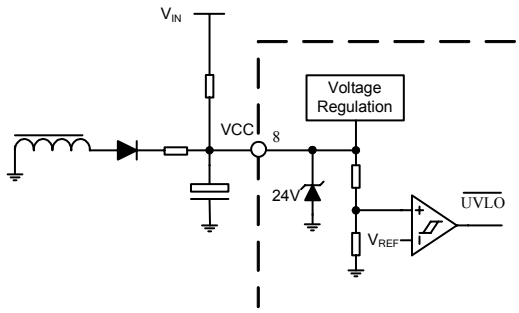

Figure 2. Supply Block

Error Amplifier

The error amplifier regulates the PFC output voltage. The internal reference on the non-inverting input of the error amplifier is 2.5V. The error amplifier's inverting input (INV) is connected to an external resistor divider which senses the output voltage. The output of the error amplifier is one of the two inputs of multiplier. A compensation loop is connected outside between the INV and the error amplifier output. Normally, the compensation loop bandwidth is set very low to realize a high power factor for the PFC converter.

To ensure fast over voltage protection, the internal OVP function is added. If the output over voltage occurs, excess current will flow into the output pin of the error amplifier through the feedback compensation capacitor. (see Figure 3) The AP1662 monitors the current flowing into the error amplifier output pin. When the detected current is higher than 40μA, the dynamic OVP is triggered. The IC will be disabled and the driver signal will be stopped. If the output over voltage lasts so long that the output of the error amplifier goes below 2.25V, static OVP will take place. Also the IC will be disabled until the error amplifier returns to its linear region.

R1 and R2 (see Figure 3) will be selected as below:

$$\frac{R1}{R2} = \frac{Vo}{2.5V} - 1 \qquad R1 = \frac{\Delta V_{OVP}}{40\mu A}$$

Pin 2 (COMP) is the output of the error amplifier. A feedback low bandwidth compensation network is

placed between this pin and the INV (pin 1) to avoid output voltage ripple influence to the system.

In the simplest case, this compensation is just a capacitor, which provides a low frequency pole as well as a high DC gain. A simple method to define the capacitance value is to provide about 20dB attenuation at twice line frequency (100Hz):

$$C_{COMP} = \frac{10}{2\pi \cdot R1}$$

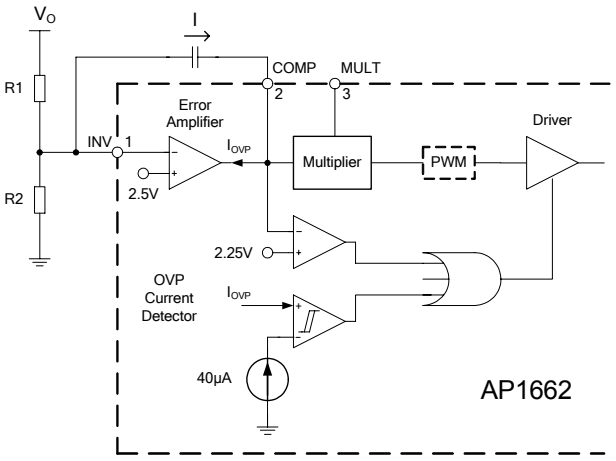

Figure 3. Error Amplifier and OVP Block

Zero Current Detection (Figure 4)

AP1662 is a DCM boundary conduction current mode PFC controller. Usually, the zero current detection (ZCD) voltage signal comes from the auxiliary winding of the boost inductor. When the ZCD pin voltage decreases below 1.6V, the gate drive signal becomes too high to turn on the external MOSFET. 500 mV of hysteresis is provided to avoid false triggering.

The boost inductor winding turn ratio, m, should be selected to ensure ZCD pin voltage is higher than 2.1V during MOSFET turned-off. Then

$$m \le \frac{V_O - \sqrt{2} \cdot V_{INRMS(MAX)}}{2.1}$$

A resistor is placed between the auxiliary winding and ZCD pin to limit the current sink to the IC. The limiting resistor's actual value can be fine-tuned to make the turn-on of the MOSFET occur exactly on the

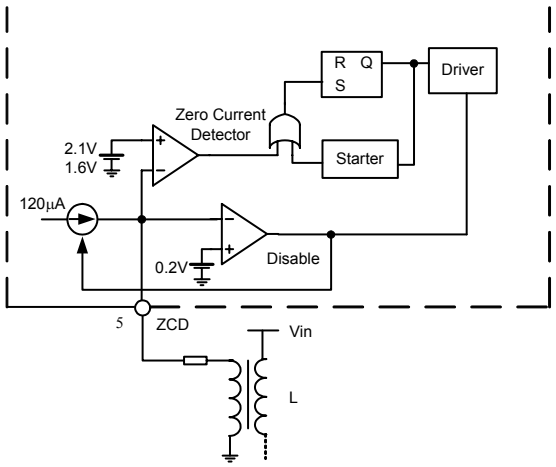

Figure 4. Zero Current Detection, Triggering and Disable Block

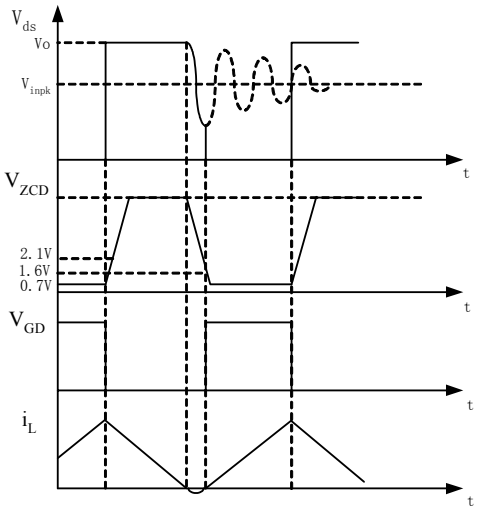

Figure 5. Optimum MOSFET Turn-on

valley of the drain voltage oscillation (When the boost inductor current reaches zero, the inductor will oscillate with the MOSFET drain capacitance. (see Figure 5)). This will minimize the MOSFET power dissipation when turned-on.

An internal starter generates a pulse to the gate of the MOSFET at first start-up. The frequency of the pulse is about 14 kHz.

If the ZCD pin is driven by an external signal, the

AP1662 will be synchronized to (the negative-going edges of) that signal. If left floating, the AP1662 will work at the frequency of its internal starter.

The ZCD pin can be used for disabling the IC. Making its voltage below 0.15V or short to the ground will disable the device thus reducing the IC supply current consumption.

Multiplier Block (Figure 6)

The multiplier has two inputs. One (Pin 3) is the divided AC sinusoidal voltage which makes the current sense comparator threshold voltage vary from zero to peak value. The other input is the output of the error amplifier (Pin 2). In this way, the input average current wave will be sinusoidal as well as reflect the load status. Accordingly, a high power factor and low THD are achieved. The multiplier transfer character is designed to be linear over a wide dynamic range, namely, 0 V to 3V for Pin 3 and 2.0 V to 5.8 V for Pin 2. The relationship between the multiplier output and inputs is described as the following equation:

$$V_{CS} = k \times (V_{COMP} - 2.5) \times V_{MULT}$$

where V_{CS} (Multiplier output) is the reference for the current sense, k is the multiplier gain, V_{COMP} is the voltage on pin 2 (error amplifier output) and V_{MULT} is the voltage on pin 3.

Figure 7 shows the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed to be in the range of 0 to 3V of V_{MULT} and 0 to 1.6V of V_{CS}.

V_{MULTpk}, the peak value for V_{MULT}, will occur at maximum mains voltage, should be 3V or below. The MULT pin resistor divider (see Figure 6) will be as follows:

$$\frac{R4}{R3+R4} = \frac{V_{MULTpk}}{\sqrt{2} \cdot V_{INRMS(MAX)}}$$

The AP1662 is equipped with a special circuit that reduces the AC input current conduction dead-angle near the zero-crossings of the line voltage (crossover distortion). In this way the THD (Total Harmonic Distortion) of the current is considerably reduced.

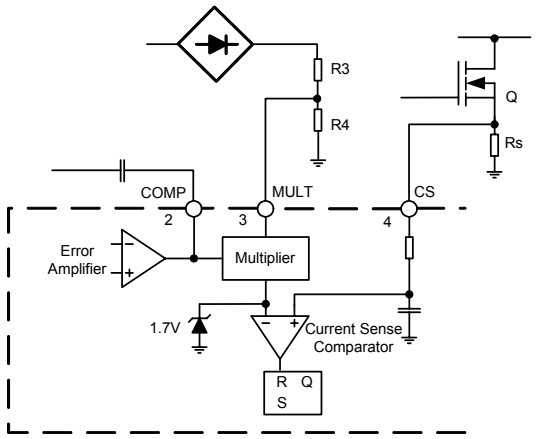

Figure 6. Multiplier Block

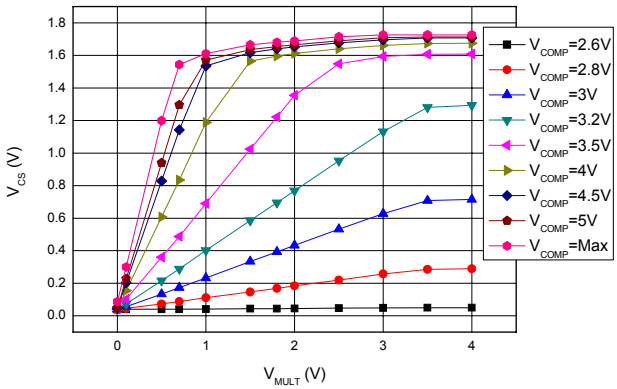

Figure 7. Multiplier Characteristics Family

Current Comparator and PWM Latch (Figure 6)

The PFC switch's turn-on current is sensed through an external resistor in series with the switch. When the sensed voltage exceeds the threshold voltage (the multiplier output voltage), the current sense comparator's output will become low and the external MOSFET will be turned off. This ensures a cycle-by-cycle current mode control operation.

The sense resistor value is calculated as follows:

$$R_S \le \frac{V_{CSpk}}{I_{CSpk}}$$

where V_{CSpk} is the maximum voltage of V_{CS}, can be set 1.6V for linear operation in the entire working range. The maximum current sense reference is 1.8V. The maximum value usually occurs during the startup process or abnormal conditions such as short load.

When the power MOSFET is turned on, a narrow spike on the leading edge of the current waveform can usually be observed. There is an internal R/C filter in AP1662 to attenuate this noise and prevent the false triggering caused by the turn-on spike. In low power applications, the external R/C filter connected to the CS pin is not needed.

Driver

The AP1662 totem pole output stage is capable of driving a Power MOSFET or IGBT with 600mA source current and 800mA sink current.

GND

Pin 6 is the Ground of the IC. This pin acts as the current return both for the internal circuitry signal and for the gate drive current. These two paths should be laid out separately in the printed circuit board.

5. Boost Circuit Basic Design

The most popular power factor correction topology is the Boost circuit. The boost converter consists of a boost inductor (L), a controlled power switch (Q), a diode (D), an output capacitor (C_O) and a control circuit (see Figure 8).

The goal of the PFC is to shape the input current in a sinusoidal waveform, in-phase with the input sinusoidal voltage.

To do this, the AP1662 uses the so-called DCM boundary Conduction Mode technique. Figure 9 shows the inductor current waveform and MOSFET gate drive signal. During a line frequency period, the turn-on time of MOSFET is kept constant, thus the inductor peak current is in track with input sinusoidal voltage waveform. When MOSFET turns off, the inductor current will decrease. Just after the inductor current reaches zero, MOSFET will turn on again.

Boost Inductor

Through the following calculation, the instantaneous switching frequency along a line cycle equation can be found:

$$f_{sw}(\theta)=\frac{(V_O-\sqrt{2}\cdot V_{INRMS}\cdot\sin(\theta))\cdot V_{INRMS}^2\cdot\eta}{2\cdot L\cdot P_O\cdot V_O}$$

The switching frequency will be at the minimum level at the top of the sinusoid and at the maximum level at the zero crossings of the line voltage. Figure 10 shows an example of the switching frequency changing during the half line cycle.

The absolute minimum frequency $f_{SW(MIN)}$ can occur at either the maximum or the minimum mains voltage. Thus the inductor value is defined by:

$$L=\frac{(V_O-\sqrt{2}\cdot V_{INRMS})\cdot V_{INRMS}^2\cdot\eta}{2\cdot f_{SWMIN}\cdot P_O\cdot V_O}$$

where V_{INRMS} can be either $V_{INRMS(MIN)}$ or $V_{INRMS(MAX)}$. The lower value for L can be selected.

The suggested minimum switching frequency is greater than the frequency of the internal starter (15kHz) to ensure a correct DCM boundary Conduction Mode operation.

The maxim inductor current is:

$$I_{LMAX\_pk}=\frac{2\sqrt{2}\cdot V_O\cdot I_O}{\eta\cdot V_{INRMS(MIN)}}$$

By AP method, we can select a type of core. Then the inductor primary turns can be calculated according

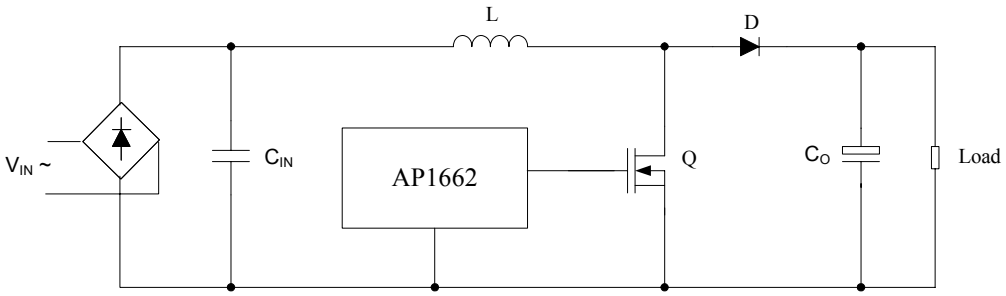

Figure 8. Boost Converter Circuit

to the following methods:

$$N = \frac{L \cdot I_{LMAX\_PK}}{B\max \cdot A_E}$$

To select Bmax according to characteristics of ferrite core and margin consideration of saturation flux density.

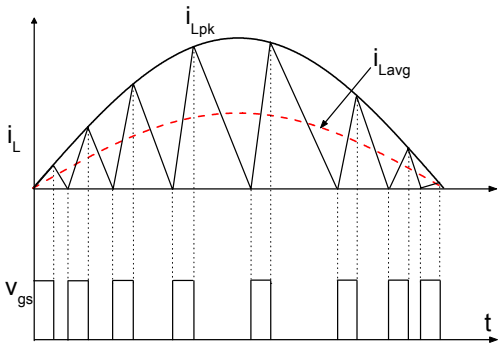

Figure 9. Boost Inductor Current in DCM Boundary Conduction Mode

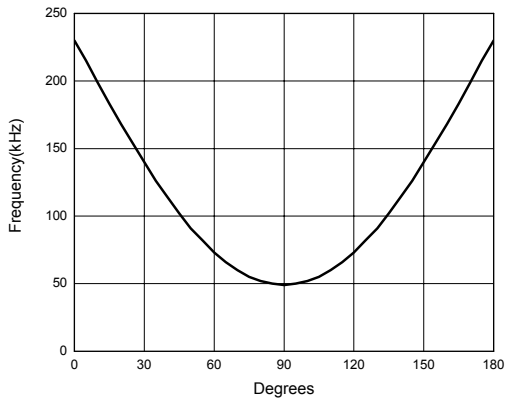

Figure 10. Switching Frequency in Half Line Cycle

Output Capacitor

The output bulk capacitor (C_O) selection depends on the DC output voltage, the allowed overvoltage, the output voltage ripple and ripple current on the capacitor.

To achieve a high power factor, the output voltage feedback control loop is slow. As a result, there is twice the mains frequency voltage ripple across the output capacitor. In addition, a high frequency ripple will appear on the ESR of the output capacitor due to Boost converter switching.

$$\Delta V_O = I_O \cdot \sqrt{\frac{1}{(4\pi \cdot f_{AC} \cdot C_O)^2} + ESR_{CO}^2}$$

With a low ESR capacitor,

$$C_O \geq \frac{P_O}{4\pi \cdot f_{AC} \cdot C_O \cdot \Delta V_O}$$

If the load is resistive, the ripple current of the output capacitor is:

$$I_{CO(RMS)} = \sqrt{\frac{32\sqrt{2} \cdot P_O^{\,2}}{9\pi \cdot \eta^2 \cdot V_{INRMS} \cdot V_O} - (\frac{V_O}{R_O})^2}$$

6. Layout Considerations

There are some considerations when laying out the PCB of the PFC circuit.

The power switching circuit loop should be as small as possible. In Boost circuit, when MOSFET turns on, there is a current flow loop including a rectifying bridge, Boost inductor and MOSFET. When the MOSFET turns off, the current flow loop includes the Boost inductor, diode and output capacitor. The two loops should be small to avoid high frequency radiation noise.

The connection between the power and signal GND should be a single point connection. Common connection of GND will introduce disturbances to small signals. Figure.11 shows the ideal ground connection diagram. The power ground and signal ground should be separated. The IC ground (GND) should connect directly to the power ground of the PFC MOSFET current sense resistor; the shorter the track is, the better the IC works. The V_{CC} capacitor C2 and C3 should be placed close to pin 8 to ensure good noise suppression.

The drain of the MOSFET has high dv/dt when switching. The control circuit including AP1662 should be kept away from it. If the MOSFET sticks to a heat sink, the heat sink should be connected to the power GND.

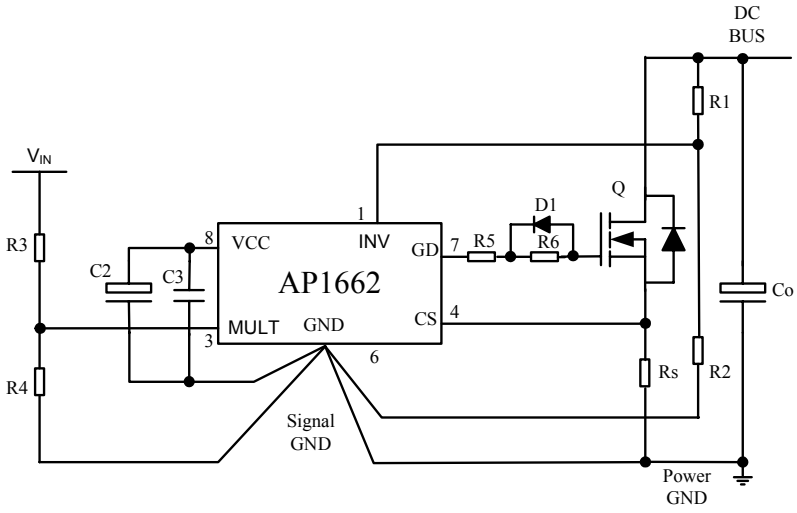

Figure 11. Correct GND Connection for AP1662 in PCB